PATENT COOPERATION TREATY

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INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

(Chapter II of the Patent Cooperation Treaty)

(PCT Article 36 and Rule 70)

Applicant's or agent's file reference XA1731	FOR FURTHER ACTION	See Form PCT/IPEA/416
International application No. PCT/GB2004/002600	International filing date *(day/month/year)* 18.06.2004	Priority date *(day/month/year)* 27.06.2003
International Patent Classification (IPC) or national classification and IPC H03K3/289		
Applicant BAE SYSTEMS PLC et al.		

1. This report is the international preliminary examination report, established by this International Preliminary Examining Authority under Article 35 and transmitted to the applicant according to Article 36.
2. This REPORT consists of a total of 4 sheets, including this cover sheet.
3. This report is also accompanied by ANNEXES, comprising:
   a. ☐ *sent to the applicant and to the International Bureau)* a total of sheets, as follows:
      ☐ sheets of the description, claims and/or drawings which have been amended and are the basis of this report and/or sheets containing rectifications authorized by this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions).
      ☐ sheets which supersede earlier sheets, but which this Authority considers contain an amendment that goes beyond the disclosure in the international application as filed, as indicated in item 4 of Box No. I and the Supplemental Box.
   b. ☐ *(sent to the International Bureau only)* a total of (indicate type and number of electronic carrier(s)) , containing a sequence listing and/or tables related thereto, in computer readable form only, as indicated in the Supplemental Box Relating to Sequence Listing (see Section 802 of the Administrative Instructions).

4. This report contains indications relating to the following items:

- ☒ Box No. I Basis of the opinion
- ☐ Box No. II Priority
- ☐ Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- ☐ Box No. IV Lack of unity of invention
- ☒ Box No. V Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
- ☐ Box No. VI Certain documents cited
- ☐ Box No. VII Certain defects in the international application
- ☐ Box No. VIII Certain observations on the international application

Date of submission of the demand	Date of completion of this report
26.04.2005	14.09.2005
Name and mailing address of the international preliminary examining authority: European Patent Office D-80298 Munich Tel. +49 89 2399 - 0 Tx: 523656 epmu d Fax: +49 89 2399 - 4465	Authorized Officer Kassner, H Telephone No. +49 89 2399-7617

INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

International application No.
PCT/GB2004/002600

Box No. I Basis of the report

1. With regard to the **language**, this report is based on the international application in the language in which it was filed, unless otherwise indicated under this item.

   ☐ This report is based on translations from the original language into the following language , which is the language of a translation furnished for the purposes of:
   - ☐ international search (under Rules 12.3 and 23.1(b))
   - ☐ publication of the international application (under Rule 12.4)
   - ☐ international preliminary examination (under Rules 55.2 and/or 55.3)

2. With regard to the **elements*** of the international application, this report is based on *(replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to this report)*:

Description, Pages	
1-5	as originally filed
Claims, Numbers	
1-3	received on 12.05.2005 with letter of 26.04.2005
Drawings, Sheets	
1/5-5/5	as originally filed

☐ a sequence listing and/or any related table(s) - see Supplemental Box Relating to Sequence Listing

3. ☐ The amendments have resulted in the cancellation of:
   - ☐ the description, pages
   - ☐ the claims, Nos.
   - ☐ the drawings, sheets/figs
   - ☐ the sequence listing *(specify)*:
   - ☐ any table(s) related to sequence listing *(specify)*:

4. ☐ This report has been established as if (some of) the amendments annexed to this report and listed below had not been made, since they have been considered to go beyond the disclosure as filed, as indicated in the Supplemental Box (Rule 70.2(c)).
   - ☐ the description, pages
   - ☐ the claims, Nos.
   - ☐ the drawings, sheets/figs
   - ☐ the sequence listing *(specify)*:
   - ☐ any table(s) related to sequence listing *(specify)*:

* *If item 4 applies, some or all of these sheets may be marked "superseded."*

Box No. V Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Yes:	Claims	1-3
	No:	Claims	
Inventive step (IS)	Yes:	Claims	1-3
	No:	Claims	
Industrial applicability (IA)	Yes:	Claims	1-3
	No:	Claims	

2. Citations and explanations (Rule 70.7):

see separate sheet

This invention relates to components for electronic latch circuits.

Object of the invention is to improve the operating frequency range of latch circuits.

Document D1 (=US-B1-6452433) discloses a latch circuit (D1, fig. 11 ref. 1100) with a first latch portion including a first clock transistor (D1, col. 11, line 24 ; D1, fig. 11 ref 1112); and a second latch portion including a second clock transistor (D1, col. 11, lines 24-25 ; D1, fig. 11 ref. 1114); wherein the first and second clock transistors form a transistor clock pair (D1, col. 11, lines 23-24) and the first clock transistor has a different emitter area than the second clock transistor (D1, col. 11, lines 27-31) .

Document D1 suggests a transistor clock pair in which the emitter of the first clock transistor is smaller than the emitter of the second clock transistor (D1, col. 11, lines 27-31). The problem to be solved in D1 is to improve the stability of the circuit without a substantial increase in operating power (D1, abstract first phrase).
The invention on the other hand according to the characterizing portion of independent claim 1 defines that the first clock transistor has a greater emitter area than the second clock transistor - therefore the "hold period/follow period" ratio being explicitly greater than 1 to increase the operating frequency range of the latch circuit; this is not shown or rendered obvious by the available prior art documents.

CLAIMS:

1. A latch circuit including:-

a first latch portion including a first clock transistor; and

a second latch portion including a second clock transistor, the first and second clock transistors forming a transistor clock pair and each of the clock transistors receiving complementary clock inputs to define a 'hold period/follow period' ratio for the transistor clock pair, the first clock transistor having a different emitter area to that of the second clock transistor;

characterised in that the emitter area of the first clock transistor is greater than that of the second clock transistor such that the 'hold period/follow period' ratio of the transistor clock pair is greater than 1.

2. A latch circuit according to claim 1, wherein the emitter area of the first clock transistor is double that of the second clock transistor.

3. A prescaler circuit including a first and second latch circuit according to claim 1 or 2.